What is claimed is:

1. A circuit comprising:

a receiver to receive a transfer signal; and

a signal detector connected to the receiver to generate an internal signal based on the transfer signal, wherein the signal detector is configured to hold the internal signal at a first signal level when the transfer signal repeatedly switches between the first signal level and a second signal level, and wherein the signal detector is configured to hold the internal signal at the second signal level when the transfer signal stops switching.

2. The circuit of claim 1, wherein signal detector includes a detect circuit to detect for changes in voltage levels represented by the transfer signal.

3. The circuit of claim 2, wherein signal detector further includes a switching circuit to switch the internal signal between the first and second signal levels.

4. The circuit of claim 3, wherein signal detector further includes a holding circuit to hold the internal signal at one of the first and second signals.

5. An integrated circuit comprising:

a plurality of terminals;

a number of transmitters connected to the terminals to transmit signals;

a number of receivers connected to the terminals to receive signals; and

a signal detector connected to at least one of the receivers to control an internal signal based on a transfer signal received by one of the receivers, wherein the signal detector is configured to switch the internal signal from a first signal level to a second signal level when the transfer signal repeatedly switches between the first and second signal levels, and wherein the signal detector is configured to

switch the internal signal from the second signal level back to the first signal level when the transfer signal stops switching.

6. The integrated circuit of claim 5, wherein the transmitters and the receivers are configured to transfer data via the terminals according to peripheral component interconnect (PCI) express standard.

7. The integrated circuit of claim 5, wherein the transmitters and the receivers are configured to transfer data via the terminals according to serial digital video output (SVDO) standard.

8. The integrated circuit of claim 5, wherein the transmitters and the receivers are configured to transfer data via the terminals according both a peripheral component interconnect (PCI) express standard and a serial digital video output (SDVO) standard.

9. The integrated circuit of claim 5 further comprising a transmitting circuit, the transmitting circuit including:

an input node to receive a send signal having the first and second signal levels; and

an output node to transfer the transfer signal to one of the terminals, wherein the transmitting circuit is configured to hold the transfer signal at one of the first and second signal levels when the send signal has the first signal level, and wherein the transmitting circuit repeatedly switches the transfer signal between the first and second signal levels when the send signal has the second signal level.

10. A system comprising:

a plurality of connectors, each of the connectors including a number of pins; and

a chipset including a chipset interface connected to at least one of the

connectors, the chipset interface including:

a plurality of terminals connected to at least one of the connectors;

a plurality of transmitters connected to the terminals, at least one of the transmitters is configured to transmit output differential signals;

a plurality of receivers connected to the terminals, at least one of the receivers is configured to received input differential signals; and

a signal detector connected to at least one of the receivers to hold an internal signal at a first signal level based on a presence of a repeated switching of a transfer signal among the input differential signals, and to hold the internal signal at a second signal level based on an absence of the repeated of switching of the transfer signal.

11. The system of claim 10, wherein one of the connectors is configured to transfer signals according to peripheral component interconnect (PCI) express standard.

12. The system of claim 10, wherein one of the connectors is configured to transfer signals according to serial digital video output (SDVO) standard.

13. The system of claim 10, wherein the interface of the chipset is configured to drive a digital display monitor.

14. The system of claim 10 further comprising a card having a number of pins connected to one of the connectors.

15. The system of claim 14, wherein the card includes a transmitting circuit, the transmitting circuit including:

an input node to receive a send signal having a first signal level and second signal level; and

an output node connected to one of the pins of the card to transfer the transfer signal to one of the pins, wherein the transmitting circuit is configured to create the presence of the repeated switching of the transfer signal when the send signal has the first signal level, and to create the absence of the repeated switching of the transfer signal when the send signal has the second signal level.

16. The system of claim 10 further comprising a motherboard in which the connectors and the chipset are located.

17. The system of claim 10 further comprising a processor connected to one of the connectors.

18. A method comprising:

monitoring a transfer signal;

holding an internal signal at a first signal level when the transfer signal stays at one of the first signal level and a second signal level;

holding the internal signal at a second signal level when the transfer signal repeatedly switches between the first and second signal levels; and

switching the internal signal from the second signal level to the first signal level when the transfer signal stops switching.

19. The method of claim 18 further comprising:

holding the internal signal at the first signal level after transfer signal stops switching.

20. The method of claim 18, wherein monitoring includes detecting for changes in signal levels of the transfer signal.

21. The method of claim 18, wherein one of the first signal level and the second signal level represents one of a voltage level and ground.

22. The method of claim 18, wherein the transfer signal is generated based on a send signal, wherein each of send signal and the internal signal has a frequency lower than the frequency of the transfer signal.

23. The method of claim 22, wherein the transfer signal repeatedly switches between the first and second signal levels when the send signal has the first signal level.

24. The method of claim 23, wherein the transfer signal stops switching when the send signal level has the second signal level.

25. The method of claim 24, wherein send signal and the internal signal have the same frequency.

26. The method of claim 18, wherein holding the internal signal at the first signal level occurs when the transfer signal stays at one of the first and second signal levels for a time interval equal to at least one cycle of the transfer signal.

27. The method of claim 26, wherein holding the internal signal at the second signal level occurs when the transfer signal repeatedly switches between the first and second signal levels such that the transfer signal has at least two consecutive cycles.